#23 / Appeal Brief Faxed 1/30/03

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Trung T. Doan

Serial No.: 09/506,204

Filed: February 17, 2000

For: CONTACT/VIA FORCE FILL TECHNIQUES AND RESULTING STRUCTURES

Confirmation No.: 6685

Examiner: T. Quach

Group Art Unit: 2814

Attorney Docket No.: 2269-3025.1US (95-1003.1)

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BRIEF ON APPEAL

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in TRIPLICATE pursuant to 37 C.F.R. § 1.192(a) and in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c):

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(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., assignee of the pending application as recorded with the United States Patent and Trademark Office in an Assignment to Micron Technology recorded on September 3, 1998, at Reel 9448, Frames 0199.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellant, Appellant's representative, nor Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF CLAIMS

Claims 1-44 stand rejected.

No claims are allowed.

The rejections of claims 1-44 are being appealed.

(4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection in the Final Office Action mailed June 5, 2002.

(5) SUMMARY OF THE INVENTION

The present invention is directed to improved semiconductor devices and structures produced by an improved method for completely filling contact holes or vias of the semiconductor devices and the resulting structures. (Specification, page 4, lines 26-27; Figs. 3-6). The improved semiconductor devices and structures are made by inserting a semiconductor wafer or other semiconducting material substrate, having one or more contact holes or vias formed in an insulating layer overlying a wafer substrate, into a high-pressure heated chamber. (Specification, page 4, line 27 to page 5, line 1). A low-melting point base layer of aluminum material is then deposited over the insulating layer and into the contact holes or vias. (Specification, page 7, lines 9-23). Once deposition is completed and while maintaining the temperature elevated, the chamber is pressurized to force the aluminum material into the contact holes or vias and thus completely eliminate voids present therein under the aluminum material base layer. (Specification, page 7, lines 9-12). A second layer of material, formed from a metal or alloy to be used as a dopant source, is then deposited over a top surface of the deposited aluminum material base layer and allowed to diffuse into the aluminum material base layer in order to form a substantially homogenous aluminum alloy within the contact hole or via. (Specification, page 9, lines 26 to page 10, lines 7; Figs. 4-5). The resulting, substantially homogeneous aluminum alloy bridges across the contact holes without exhibiting any deformation. (Fig. 5). In other words, the resulting homogeneous aluminum alloy does not extrude inward toward the contact hole.

The newly formed homogenous aluminum alloy possesses the desirable characteristics of high melting-point aluminum alloys, but without the associated difficulties and disadvantages of depositing such alloys in their preformed state. (Specification, page 10, lines 4-7; Fig. 5). Formation of the homogenous aluminum alloy within the contact holes or vias of the wafer improves the strength, stress migration, and electromagnetic properties of the contacts or vias in a viable, economical manner easily applied to existing fabrication methodologies. (Specification, page 5, lines 14-17).

(6) ISSUE

A. Whether claims 1-44 are unpatentable under 35 U.S.C. § 103 as being obvious in view of Saran et al. in combination with Kobayashi et al.

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

A. With respect to issue A, claims 1-44 stand or fall together.

(8) ARGUMENT

A. Standard of Patentability Under 35 U.S.C. § 103(a)

Applicants note that a proper rejection of claims under 35 U.S.C. § 103(a) requires that the Patent and Trademark Office (hereinafter "the Office") must first establish a prima facie case of obviousness. M.P.E.P. § 2142. The standard for establishing a prima facie case of obviousness is set forth in M.P.E.P. 706.02(j) where it states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

With regard to combining references for a rejection under 35 U.S.C. § 103(a) there are additional issues that the Office must consider. According to the M.P.E.P. "[a] prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." M.P.E.P. § 2141.02 (citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 421 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984)). Additionally, "[i]t is improper to combine references where the references teach away from their combination." M.P.E.P. § 2145(X)(D)(2) (citing *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)).

In view of these standards, and the arguments set forth below, Applicants respectfully submit that the Office has not established a prima facie case of obviousness under 35 U.S.C. § 103(a).

B. Patentability of Claims 1-44

In an Office Action mailed on June 5, 2002, and made Final (hereinafter "the Final Action"), the Examiner rejected claims 1-44 under 35 U.S.C. § 103 as being obvious over U.S. Patent No. 5,998,296 to Saran et al. (hereinafter "Saran") in view of U.S. Patent No. 4,941,032 to Kobayashi et al. (hereinafter "Kobayashi").

Applicant submits that the 35 U.S.C. § 103(a) rejection is improper and traversed because Saran and Kobayashi do not teach or suggest all of the claim limitations and because there is no motivation or suggestion to combine the cited references. Specifically, Saran and Kobayashi do not teach or suggest three limitations in independent claims 1, 23, and 39. The cited references do not teach or suggest contact holes being completely filled with a homogeneous aluminum alloy (i.e. void-free); a nondeformed aluminum bridge over the contact holes; and the

homogeneous aluminum alloy being in direct contact with a substrate. Further, the Saran and Kobayashi references cannot be properly combined since they teach away from each other.

Independent claims 1, 23 and 39 of the present invention recite a semiconductor assembly having a void-free, aluminum alloy-containing material within contact holes in an insulating layer, in direct contact with a substrate, and having a nondeformed aluminum bridge over the contact holes. This product is created by depositing an aluminum material on an exposed surface of the insulating layer, heating the aluminum material to partially fill the holes, applying pressure to the aluminum material to completely fill the holes, depositing a different metal material over the contact holes and forming a homogeneous metal fill material in the contact holes and a nondeformed aluminum bridge over the contact hole. This process creates a different product than that described in Saran.

If "the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim." M.P.E.P. § 2111.02 (citing *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165-66 (Fed. Cir. 1999)). The preamble of independent claims 1, 23, and 39 clearly recites structural limitations that distinguish over Saran and Kobayashi imparting patentability to them. Dependent claims 2-22, 24-38, and 40-44 are all novel and nonobvious since they depend from and contain all of the limitations of novel and nonobvious independent claims. M.P.E.P. § 2143.03 (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)).

As stated in the specification of the present invention, this application alleviates the problems of voids being formed inside each hole below the filled or bridged mouth. (Specification, page 5, lines 4-7). Significantly, as stated above, the present invention also includes formation of an aluminum bridge over the hole or via that is not deformed or extruded inwardly. The present invention overcomes the limitations present in the product described in Saran, namely a semiconductor device structure having voids formed inside each contact hole and having an aluminum bridge over the contact hole that is deformed inward toward the contact hole.

Applicant submits that Saran does not teach or suggest the contact holes being "void-free". In the Final Action, the Examiner maintains that Saran teaches the "void-free" feature in Figs. 1B and 2B. (Final Action, page 3). While the Figs. 1B and 2B appear to show the contact holes being completely filled by the aluminum material, Figs. 1B and 2B must be interpreted in view of the specification. Saran "must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." M.P.E.P. § 2141.02 (citing *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 421 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984)). Applicant respectfully disagrees with the Examiner's reading of Saran and specifically points out that the description of these figures describes applying pressure that "forces the fill metal to descend into opening 20 and substantially fills the void therein." (Emphasis added, Saran, column 3, lines 3-5 and lines 37-39). While the fill metal substantially fills the void therein of opening 20, Saran does teach or suggest completely filling the void (i.e. being void-free) as in the present invention.

Applicant further submits that Saran does not teach or suggest a nondeformed aluminum bridge over the contact hole. The Examiner also contends that "the non-deformed aluminum bridge is clearly met by Saran as shown in Fig. 2B, wherein no deformation is shown." (Final Action, page 3). Applicant respectfully submits that Fig. 2B must be read in view of its description in the specification of Saran. Applicant disagrees with this contention as well, since Saran teaches first forming a fill metal layer over the semiconductor, forming a surface coating over the metal fill layer and then applying high pressure on the surface coating to force the fill metal into the opening. (Saran, column 1, lines 55 to 61 and column 2, line 50 to column 5, line 5). After the formation of surface coating layer 32, pressure exerted on the surface coating layer "forces the fill metal to descend into opening 20." (Id. at col. 3, lines 1-5). With specific reference to Fig. 2B, Saran teaches that pressure exerted on the surface coating layer "forces the fill metal to descend into opening 50." (Id. at col. 3, lines 36-39). As a result, the process described in Saran to partially fill the contact holes results in an aluminum bridge that is deformed or extruded inwardly. Fig. 2 of the Applicant's patent application illustrates the product made by the process disclosed in Saran. In contrast to Saran, the forced fill process of the present invention completely and evenly fills all of the contact holes, thus creating a distinguishable and novel product. When the figures in Saran are interpreted correctly in view of their description in the specification, it is clear that a nondeformed aluminum bridge is not taught or suggested.

Applicant submits that Saran fails to teach or suggest the homogeneous aluminum alloy material being in direct contact with a substrate. Saran teaches deposition of barrier/adhesion

layers 22/24 and 52/54 between the fill metal layer (30/60) and the substrate (18/48), which is contrary to the recitations of the pending claims in the present invention. The present invention eliminates the need for deposition of barrier/adhesion layers in order to conserve the target material composition. (Specification, page 8, lines 14-20). This results in semiconductor assemblies and devices having an aluminum alloy-containing material that is in direct contact with the underlying substrate and which does not require the existence of a barrier/adhesion layer between the aluminum alloy and the substrate. Thus, the present invention results in a semiconductor assembly or device having an aluminum alloy-containing material in direct contact with a substrate and having a nondeformed aluminum bridge over the completely filled contact holes, which is designed to overcome the limitations of Saran. Accordingly, Saran merely recites the shortcomings of prior art structures and, thus, teaches away from the present invention.

In response to this issue in the Final Action, the Examiner maintains that because Saran states that a barrier may be included (but is not required), direct contact would have been obvious between the alloy material and the underlying substrate. However, applicant respectfully notes that all the claimed limitations must be met and that Saran does not describe a single embodiment with all of the claimed limitations that also exclude the barrier layer. Stated differently, Saran does not include a single embodiment lacking the barrier layer and including a void-free, homogeneous aluminum alloy material within contact holes in an insulating layer, in direct contact with a substrate and having a nondeformed aluminum bridge over the contact

holes. As discussed hereinafter, Kobayashi does not supplement the deficiencies in the Saran reference in order to establish a *prima facie* case of obviousness.

Applicant submits that Kobayashi cannot be properly combined with Saran and disagrees with the Examiner's assessment of Kobayashi. Kobayashi teaches using an aluminum alloy as material for a metal electrode. Specifically, Kobayashi relates to amorphous silicon solar cells and pin type photosensors utilizing transparent conductive thin films that are specifically designed to avoid reduction of reflectivity. (Kobayashi column 1, lines 12-28, and column 3, lines 21-26). Kobayashi specifically defines "semiconductor device" as "a solar cell, photosensor, photosensitive drum, thin film transistor, electroluminescent device, and the like . . . ." (Id. at column 4, lines 12-16). In fact, Examples 1-6 of Kobayashi are limited to description of glass substrates and solar cells. (Id. at columns 5-6).

Applicant submits that Kobayashi cannot properly be combined with Saran because the cited references teach away from the combination. Notably, Kobayashi fails to teach using the aluminum alloy within contact holes in an insulating layer, as claimed in the present invention. The aluminum alloy of Kobayashi is used only as a metal electrode which can be electrically connected to a semiconductor. In contrast, the formation of the homogeneous aluminum alloy of the present invention is formed within the contact holes or via of the wafer thus improving strength, stress migration and electromagnetic properties of the contact or vias. Because there are no contact holes in the structure of Kobayashi, Kobayashi actually teaches away from a semiconductor structure having a homogeneous aluminum alloy with an insulating layer. There is no motivation in Kobayashi to combine any of its elements with the elements of Saran,

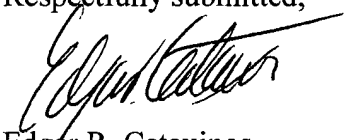
particularly when a number of elements are non-existent therein and where the inventions are drawn to two different types of inventions having different functions and operation. To combine the references as done in the Final Action constitutes impermissible reliance on hindsight reconstruction. In view of the foregoing, Applicant respectfully contends that Kobayashi and Saran strongly teach away from combining their respective teachings.

Neither Saran nor Kobayashi, either alone or in combination, teach or suggest all the claim limitations of independent claims 1, 23 and 39 of which claims 2-22, 24-28 and 40-44 subsequently depend upon. Further, Saran and Kobayashi teach away from combining their respective teachings. Therefore, the Applicant respectfully requests that the Board reverse the Examiner's obviousness rejections.

(9) APPENDIX

A copy of claims 1-44 as presently amended is appended hereto as "Appendix A."

Respectfully submitted,



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APPENDIX A

CLAIMS

1. A semiconductor device structure having a void-free, homogeneous aluminum alloy material within contact holes in an insulating layer, in direct contact with a substrate and having a nondeformed aluminum bridge over the contact holes, the semiconductor device structure formed by the method comprising:

depositing an aluminum material on an exposed surface of the insulating layer and over the contact holes;

heating the aluminum material to reflow the aluminum material into the contact holes so as to at least partially fill the contact holes;

applying pressure to the aluminum material to completely fill the contact holes;

depositing a different metal material on the aluminum material over the contact holes; and

diffusing the different metal material into the aluminum material to form a homogeneous aluminum alloy fill material in the contact holes and a nondeformed aluminum bridge over the contact holes.

2. The semiconductor device structure of claim 1, wherein depositing an aluminum material comprises physical vapor deposition of the aluminum material.

3. The semiconductor device structure of claim 1, wherein heating and applying pressure to the aluminum material are executed simultaneously.

4. The semiconductor device structure of claim 1, wherein heating the aluminum material comprises heating the aluminum material with a heater.

5. The semiconductor device structure of claim 4, wherein the aluminum material is heated to about 400°C.

6. The semiconductor device structure of claim 1, wherein heating the aluminum material comprises irradiating the aluminum material with argon plasma.

7. The semiconductor device structure of claim 1, wherein heating the aluminum material comprises simultaneously heating the aluminum material with a heater and irradiating the aluminum material with argon plasma.

8. The semiconductor device structure of claim 1, wherein applying pressure comprises introducing the semiconductor device into a high pressure chamber and pressurizing the high pressure chamber.

9. The semiconductor device structure of claim 8, further comprising maintaining the temperature within the high pressure chamber at about 400°C.

10. The semiconductor device structure of claim 8, wherein the high pressure chamber is pressurized to more than 500 atm.

11. The semiconductor device structure of claim 1, wherein depositing a different metal material comprises physical vapor deposition of the different metal material.

12. The semiconductor device structure of claim 1, wherein depositing a different metal material comprises vacuum evaporation deposition of the different metal material.

13. The semiconductor device structure of claim 1, wherein the different metal material comprises a metal alloy.

14. The semiconductor device structure of claim 1, wherein the different metal material comprises a substantially pure metal.

15. The semiconductor device structure of claim 14, wherein the substantially pure metal comprises copper.

16. (Previously Amended) The semiconductor device structure of claim 15, wherein the copper is deposited on the aluminum material through an electrolysis plating process.

17. The semiconductor device structure of claim 14, wherein the substantially pure metal comprises nickel.

18. The semiconductor device structure of claim 17, wherein the nickel is deposited on the aluminum material through an electrolysis plating process.

19. The semiconductor device structure of claim 1, wherein diffusing the different metal material comprises heating the different metal material to diffuse the different metal material into the aluminum material.

20. The semiconductor device structure of claim 19, wherein heating the different metal material comprises irradiating the different metal material with argon plasma.

21. The semiconductor device structure of claim 19, wherein heating the different metal material comprises simultaneously heating the different metal material with a heater and irradiating the different metal material with argon plasma.

22. The semiconductor device structure of claim 1, wherein diffusing the different metal material comprises annealing the different metal material to diffuse the different metal material into the aluminum material.

23. A semiconductor assembly having a void-free, homogeneous aluminum alloy material within contact holes in an insulating layer, in direct contact with a substrate and having a nondeformed aluminum bridge over the contact holes, the semiconductor assembly formed by the method comprising:

providing a semiconductor substrate having an insulating layer overlying the semiconductor substrate, the insulating layer having contact holes formed therein;

simultaneously depositing and heating an aluminum material an on outer surface of the insulating layer and over the contact holes;

applying pressure to the aluminum material to completely fill the contact holes;

depositing a different metal material on the aluminum material; and

diffusing the different metal material into the aluminum material to form a substantially homogeneous void-free, aluminum alloy fill material in the contact holes and a nondeformed aluminum bridge over the contact holes.

24. The semiconductor assembly of claim 23, wherein depositing an aluminum material comprises physical vapor deposition of the aluminum material.

25. The semiconductor assembly of claim 23, wherein heating the aluminum material comprises irradiating the aluminum material with argon plasma.

26. The semiconductor assembly of claim 23, wherein heating the aluminum material comprises simultaneously heating the aluminum material with a heater and irradiating the aluminum material with argon plasma.

27. The semiconductor assembly of claim 23, wherein applying pressure comprises introducing the semiconductor device into a high pressure chamber and pressurizing the high pressure chamber.

28. The semiconductor assembly of claim 27, further comprising maintaining the temperature within the high pressure chamber at about 400°C.

29. The semiconductor assembly of claim 27, wherein the high pressure chamber is pressurized to more than 500 atm.

30. The semiconductor assembly of claim 23, wherein depositing a different metal material comprises physical vapor deposition of the metal material.

31. The semiconductor assembly of claim 23, wherein depositing a different metal material comprises vacuum evaporation deposition of the different metal material.

32. The semiconductor assembly of claim 23, wherein the different metal material comprises a metal alloy.

33. The semiconductor assembly of claim 23, wherein the different metal material comprises a substantially pure metal.

34. The semiconductor assembly of claim 33, wherein the substantially pure metal comprises copper.

35. The semiconductor assembly of claim 34, wherein the copper is deposited on the aluminum material through an electrolysis plating process.

36. The semiconductor assembly of claim 33, wherein the substantially pure metal comprises nickel.

37. The semiconductor assembly of claim 36, wherein the nickel is deposited on the aluminum material through an electrolysis plating process.

38. The semiconductor assembly of claim 23, wherein diffusing the different metal material comprises heating the different metal material sufficiently to diffuse the metal material into the aluminum material.

39. A semiconductor assembly having a void-free, aluminum-containing material within contact holes in an insulating layer, in direct contact with a substrate and having a nondeformed aluminum bridge over the contact holes, the semiconductor assembly formed by the method comprising:

providing a semiconductor substrate having a dielectric layer overlying a semiconductor substrate, the insulating layer having contact holes extending therethrough;

filling the contact hole with a metal material including aluminum as a major constituent; and

modifying the characteristics of the metal material by diffusing at least a second metal material thereinto to form a void-free, homogeneous alloy fill material in the contact holes and a nondeformed aluminum bridge over the contact hole and a nondeformed aluminum bridge over the contact holes.

40. The semiconductor assembly of claim 39, wherein the metal material comprises an alloy containing aluminum and at least one metal selected from the group consisting of copper, silver, zinc, nickel, and tin.

41. The semiconductor assembly of claim 39, wherein the second metal material is selected from the group consisting of copper, silver, zinc, tin, nickel, and magnesium.

42. The semiconductor assembly of claim 39, wherein filling the contact hole comprises physical vapor deposition of the metal material.

43. The semiconductor assembly of claim 39, further comprising depositing at least one second metal material onto the metal material through physical vapor deposition.

44. The semiconductor assembly of claim 39 further comprising depositing at least one second metal material onto the metal material through vacuum evaporation deposition.

PATENT
Attorney Docket No. 3025.1US (95-1003.1)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Examiner:	T. Quach	Group Art Unit No.:	2814
Applicant(s):	Trung T. Doan	Filing date:	February 17, 2000
Serial No.:	09/506,204	For (title):	CONTACT/VIA FORCE FILL TECHNIQUES AND RESULTING STRUCTURES

TRANSMITTAL OF BRIEF ON APPEAL (PATENT APPLICATION — 37 C.F.R. § 192)

ATTENTION: BOARD OF PATENT APPEALS AND INTERFERENCES
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the BRIEF ON APPEAL in this application further to the Notice of Appeal filed on September 16, 2002.

2. STATUS OF APPLICATION
This application is on behalf of
- ☒ other than a small entity
- ☐ small entity
  verified statement:
  - ☐ attached
  - ☐ already filed

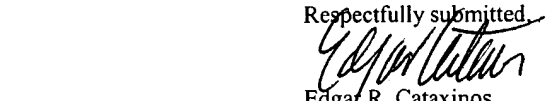
3. FEE FOR FILING APPEAL BRIEF
- ☐ small entity status $160
- ☒ other than a small entity $320

4. EXTENSION OF TIME
- ☐ A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.

5. FEE PAYMENT
- ☒ Check No. 3291 is enclosed in payment of the fee for filing the Brief on Appeal plus any extension of time for which a petition has been filed.
- ☐ Please charge the fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

Respectfully submitted,



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